Chip Design Contest

2026 IDEC Congress CDC

Design of a 32 – 40 GHz Two-Stage Cascode Low-Noise Amplifier in 28-nm CMOS

JeongSu Lee and TaeHwan Jang
Hanyang University ERICA

Introduction

This work presents a 28-nm CMOS low-noise amplifier designed for operation in the 32–40 GHz mmWave band. In a mmWave receiver, the LNA is the first amplification stage and strongly affects the overall gain, noise performance, input matching, and stability. However, at high frequencies, parasitic components of transistors and passive devices make it difficult to achieve both high gain and wide bandwidth. Therefore, this work adopts a two-stage cascode LNA structure to simultaneously achieve high gain, sufficient bandwidth, and excellent isolation.

Circuit Design

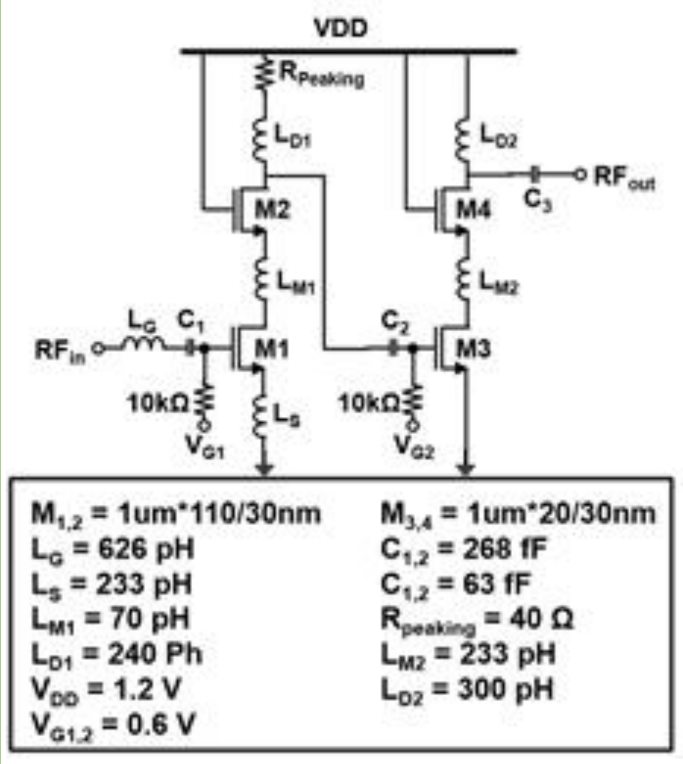

Fig 1. Schematic of the proposed LNA

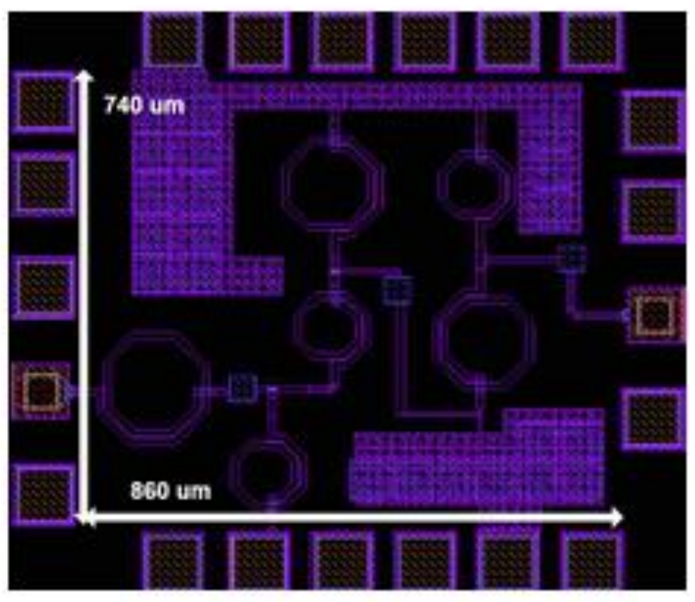

Fig 2. Layout of the proposed LNA

- A two-stage cascode structure was employed to achieve both high gain and excellent high-frequency stability. By combining the high-gain characteristic of the common-source structure with the superior isolation characteristic of the common-gate structure, the feedback between the input and output was reduced, thereby improving reverse isolation and stability.
- An interstage matching inductor was inserted between the output of the first stage and the input of the second stage. This inductor mitigates the loading effect caused by the parasitic capacitance at the second-stage gate and improves power transfer within the target frequency band. It also enables optimization of the overall frequency response by controlling the gain peak location and bandwidth.
- In the mmWave band, resonance-based matching can cause excessive gain peaking at a specific frequency or gain degradation at the band edges. To compensate for this effect, a peaking resistor was added to the drain path of the first stage. The peaking resistor controls the Q-factor of the drain load network, suppresses excessive gain peaking, and contributes to gain flattening and securing the required 3-dB bandwidth.

Results

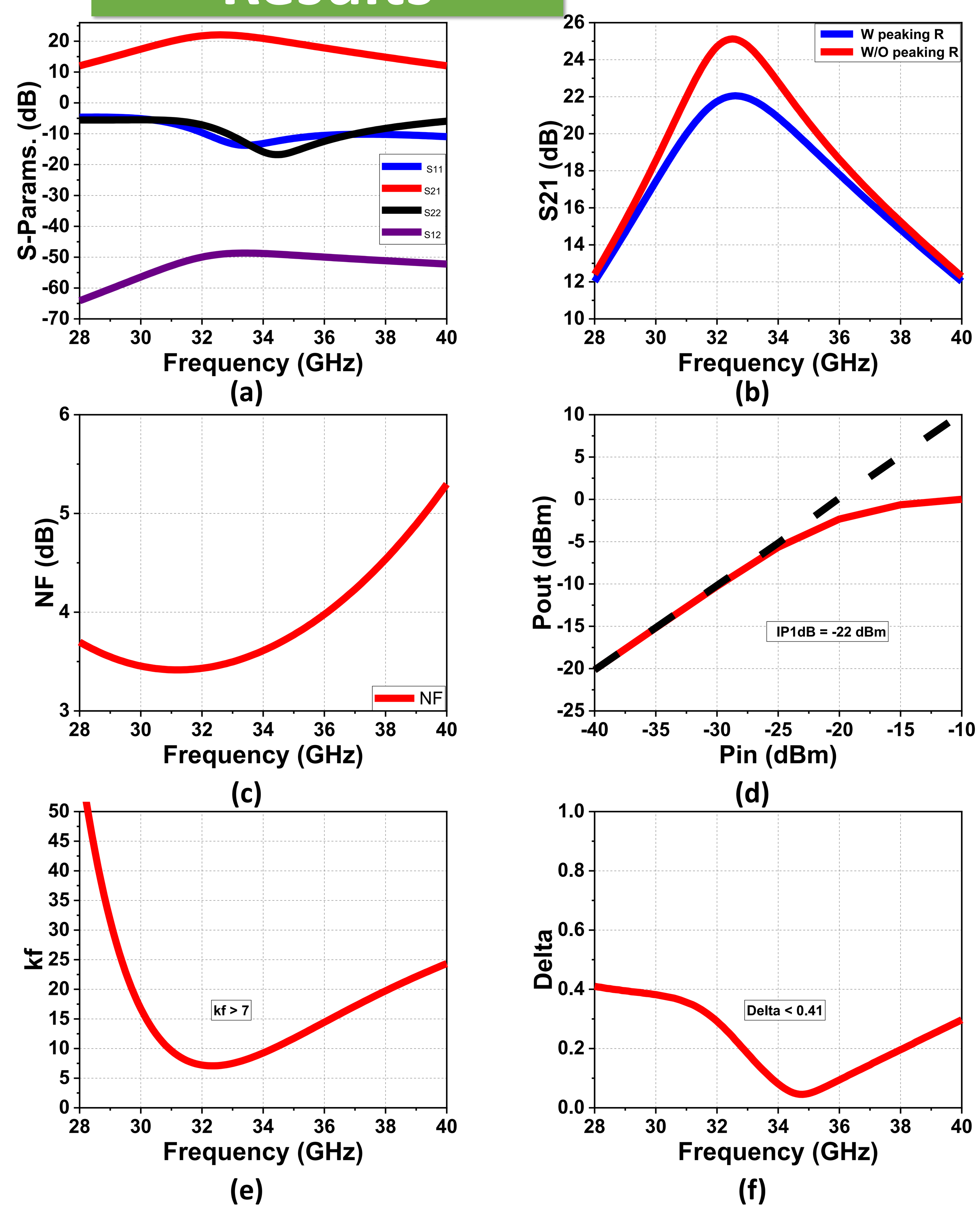

Fig 3. Simulation results of (a) S-Params., (b) gain, (c) NF, (d) P1dB, (e) kf and (f) delta

Phase Shifter Comparison Table						
Ref.	Tech.	Gain (dB)	Bandwidth (GHZ - GHz)	NF (dB)	P1dB (dBm)	Power (mW)
This Work	28nm CMOS	22.05	32 - 40	3.9	-22	14.4

As a result, the proposed LNA achieved input matching over the 32–40 GHz band, with a maximum gain of 22.05 dB. The average noise figure was 3.9 dB, and the power consumption was 14.4 mW. Excellent reverse isolation was also achieved through the cascode structure. In particular, the interstage inductor and peaking resistor effectively controlled the gain response and helped secure the required 3-dB bandwidth. Therefore, the proposed structure provides a suitable LNA design approach for high-gain, low-noise, and stable mmWave receiver front-ends around the 33 GHz band.